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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,162	11/25/2003	Atsushi Kuwata	8001-1176	4322

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YOUNG & THOMPSON  
745 SOUTH 23RD STREET  
2ND FLOOR  
ARLINGTON, VA 22202

EXAMINER
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SUN, SCOTT C

ART UNIT	PAPER NUMBER
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2182

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/720,162	<b>Applicant(s)</b> KUWATA, ATSUSHI	
	<b>Examiner</b> Scott Sun	<b>Art Unit</b> 2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 14 February 2005.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.
2. Prior to presenting new ground(s) of rejection, examiner notes that it would better clarify the rejection by first responding to applicant's remarks filed 12/14/2005.

Applicant's arguments in the remarks are summarized as:

- a. Rivard does not qualify as prior art.
  - b. Rivard does not teach newly added limitation of read/write a first data to a first disk with a timing determined in relation to read/write of a second data to a second disk.
3. Regarding argument 'a', examiner asserts that prior rejection, as applicant reasonably interpreted, was intended as 102(e), in which Rivard would qualify as prior art with an effective filing date of 10/2/2002 (provisional). If applicant challenges Rivard's qualification as prior art, specific evidence should be submitted to clearly point out what elements are missing in the provisional application from which Rivard claims priority.
4. Regarding argument 'b', examiner notes that Rivard teaches each WCC (write cache controller) can control write cache for one or more disks (paragraphs 47-48; acknowledged in page 9 of applicant's remarks). Rivard further teaches disk status data can be used for scheduling disk writes (paragraph 64). Although Rivard does not

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explicitly teach the specific scheduling technique claimed by applicant, the technique is well known in the art at the time of invention, and would be obvious for a person of ordinary skill to combine with Rivard's system. A more detailed discussion will be presented in the new rejection.

5. Further regarding argument 'b', examiner notes that applicant provided a more detailed discussion of applicant's invention (remarks, page 9), including elements that applicant argues are missing in Rivard's teachings. However, examiner reminds applicant that although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

6. The following rejections are made in light of the above discussions and in response to applicant's amended claims.

### ***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rivard (PG Pub# US2004/0078508 A1) in view of Weber (US Patent #5,596,708).

9. As per claim 1, Rivard discloses a disk array apparatus (figure 2) comprising a cache memory (data store 210) that temporarily stores data to be read from or written to disks (paragraphs 45, 54-56); Examiner notes that Rivard teaches data store 210 holds read data, and WCC, which function as a write cache and controller, can be integrated with the data store. Alternatively, WCC can be implemented to also have a read cache (paragraph 56).

Rivard further teaches a control unit (cache access concentrator 201, comprising WCC units) which associates data associated with logical addresses (block address) with physical addresses, writes the data associated with physical address in the cache memory (over-write) and processes preferentially for writing the data associated with the physical addresses (paragraphs 55, 58; 70); Examiner notes that Rivard teaches WCC uses a protocol such as SCSI or ATAPI for communication with the disks, in either case LBA (logical block address) scheme would be used. In order to communicate with the physical disk, LBA is translated (associated) with a corresponding physical disk block location, usually in terms of cylinder-head-sector. Rivard further teaches that writes to disks can be scheduled (interpreted as processing preferentially) to optimize disk efficiency.

Although Rivard teaches write scheduling and a plurality of disks, Rivard does not teach explicitly reading/writing data to a first disk with a timing determined in relation to reading/writing to a second disk. However, Weber teaches a first disk (drive a) and a second disk (drive b; figure 5), and wherein a control unit processes first data (parity) to be read from or written to said first disk with a timing determined in relation to reading or

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writing of a second data (data) to said second disk (column 8, lines 9-51). Teachings of Rivard and Weber are from the same field of disk storage systems, and specifically of read/write performance.

Therefore, it would have been obvious at the time of invention for a person of ordinary skill in the art to combine teachings of Rivard and Weber by using the read/write scheduling technique disclosed by Weber in the storage system of Rivard for the benefit of efficient utilization of the disk drives (Weber; column 8, lines 42-44).

10. As per claim 2, Rivard and Weber combined discloses the disk array apparatus as claimed in claim 1, and Rivard further teaches wherein said control unit releases the data associated with the physical addresses in the cache memory from a state in which the data is associated with the physical addresses after confirming that the writing is completed (paragraph 69).

11. As per claim 3, Rivard and Weber combined discloses the disk array apparatus as claimed in claim 1, and Rivard further teaches wherein said control unit comprises a plurality of control units (write cache controllers) which are physically independent of one another and wherein if a failure occurs in one control unit, another control unit takes over the preferential processing for the data associated with a physical address in the cache memory (paragraph 81).

12. As per claims 4-6, Rivard and Weber combined discloses the disk array apparatus as claimed in claim 1-3, wherein Rivard further teaches wherein said cache memory is a nonvolatile memory (paragraph 51, 52, 81). Examiner notes Rivard also teaches the use of NVRAM (non-volatile RAM) in prior art systems (paragraph 26).

13. As per claims 7-16, the examiner finds these claims contain the same limitations as above rejected claims 1-6. Therefore, the same arguments are applied.

14. Examiner notes that newly added claim 11 recites a narrower scope than claim 1. However, Weber still teaches each limitation. Specifically, Weber teaches new data (column 8, line 22) to be written at least to a first disk (drive b; column 8, line 22-26), and new check information (new parity; column 8, line 37) to be written at least to a second disk (drive a; column 8, lines 37-41) that is different than said first disk.

### ***Conclusion***

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Specifically, amendments made in independent claims 1 and 7 significantly changed the scope of the claims. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

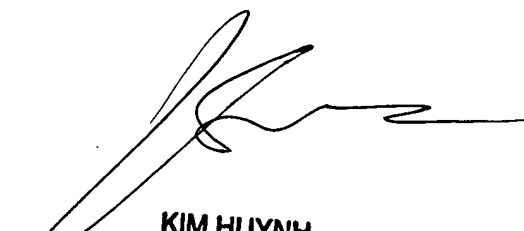
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Sun whose telephone number is (571) 272-2675. The examiner can normally be reached on M-F, 10:30am-7pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS  
2/8/2006



KIM HUYNH  
SUPERVISORY PATENT EXAMINER  
2/15/06  
KIM HUYNH  
SUPERVISORY PATENT EXAMINER